

RESEARCH ARTICLE

Reducing Switch Count in a Self-Balancing Nine-Level Switched Capacitor Inverter: A Modified Approach

Lois Anuale ^{a,*}, Osasumwen J. T. Alimikhena ^b, Olafuyi Ogunmuyiwa ^c

^aEnergy Access and Renewable Energy Technology, University of Port Harcourt, Choba, Port Harcourt 500102, Nigeria.

^bElectrical Electronics Engineering Department, University of Benin City, Benin 300213, Nigeria.

^cElectrical Electronics Engineering Department, University of Ibadan, Ibadan 200005, Nigeria.

Abstract

Renewable energy sources are becoming more and more popular to minimize environmental damage while meeting the world's expanding demand for electricity. However, components like DC-AC converters, transformer/inductor absence operation, front-end DC-DC converters with high gain capacity, and high voltage at a selected level are needed for small-scale PV solar independent AC loads and for grid applications as well as. This study offers a step-up boost inverter with quadruple operation of 9-levels that solves the problem by using a switched capacitor approach with less complications. By utilizing the control scheme itself, the topology is intended to balance capacitor voltages without the requirement for sensors. A phase disposition-pulse width modulation (PD-PWM) control technique is employed in this topology. This work focuses on the switching operation modes of the anticipated inverter and presents experimentally confirmed simulation experiments carried out in MATLAB/Simulink. All things considered; this research presents a viable option for renewable energy systems that can assist in satisfying the demand for electricity while preserving the environment.

Keywords: Multilevel inverter, Total Harmonic Distortion (THD) reduction, Switched capacitor technique, Power quality.

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1. Introduction

The global electricity demand is increasing rapidly, but the predominant means of electrical energy generation, such as the combustion of fossil fuels and nuclear materials, result in the emission of harmful gases that contribute to environmental imbalances on a global scale. To address this challenge, there is a growing interest in adopting renewable energy sources that are environmentally friendly. However, renewable energy generation stations are often situated at a considerable distance from load centers, resulting in amplified transmission and distribution losses during the delivery of electrical energy [1]–[3]. Rooftop distributed solar photovoltaic (PV) systems have been presented recently as a solution to this problem. These systems typically exhibit power and voltage ratings in the range of 0.5 kW to 5 kW and 60–100 V, respectively. Rooftop PV systems are becoming increasingly popular, and the number of units is expected to reach 100 million by 2030, which could be achieved by maintaining today's yearly installation rate. Rooftop PV systems offer numerous benefits, including reduced transmission and distribution losses, lower capital and operational costs, and lower maintenance requirements. The paper suggests a modified nine-level inverter that achieves all of the aforementioned

*Corresponding author

Email addresses: lois.david@earet.uniport.edu.ng, loisanuale@gmail.com (Lois Anuale), alimikhena@ndphc.net (Osasumwen J. T. Alimikhena), oogunmuyiwa2363@stu.ui.edu.ng (Olafuyi Ogunmuyiwa).

objectives with fewer components by using a switched capacitor approach. The topology is designed to balance capacitor voltages without the need for sensors, using the control scheme itself. A Phase disposition Pulse Width Modulation (PDPWM) is handled as the control scheme for the proposed topology. Overall, rooftop PV systems offer a promising solution for renewable energy systems that can help meet electricity demands while maintaining a clean and green environment [4].

The increasing demand for electrical energy is met by conventional energy sources, which harm the environment. To address this issue, renewable energy sources are becoming more popular. Installing distributed solar photovoltaic (PV) systems on rooftops has been a novel way to lower transmission and distribution losses when the power is transferring from various generation stations to local load centers [5]- [8]. In a step-up 9-level inverter employing a technique of switched capacitor (SC) and requires fewer components is proposed to address the challenges of rooftop PV systems. The topology is designed to balance capacitor voltages without the need for sensors, using the control scheme itself. The multilevel inverter (MLI) is a power conversion technology used in power electronics and renewable energy systems. The necessity of DC-AC conversion and high-gain DC-DC converters to match AC grid voltage levels is covered in the article. The various types, such as MLI's of diode-clamped, flying-capacitor [9]- [11], and cascaded H-bridge (CHB) [12]- [14] are also discussed along with the modifications made to lessen the reliance on isolated DC sources, address capacitor voltage balancing issues, and minimize the number of switches [15]- [18]. It is reported that the SC enabled MLIs are well-suited for RE system applications, including small scale solar PV rooftops [19].

A boost-SC inverter by arranging in a Marx structure manner that employs SC techniques to increase the number of output voltage levels [14]. The Marx structure units enhance the output voltage levels when added to the H-bridge. Other advancements in MLIs have been proposed in [16] to overcome challenges such as capacitor unbalancing, reduced switch count, and improved voltage levels. For example, a cascaded MLI using separate DC voltage sources for the front-end and back-end units has been proposed in [16]. Switched capacitor techniques are used by the front-end unit, while an H-bridge unit is used by the lateral end. The number of layers is increased by cascading these units together. Furthermore, a hybrid SC-MLI [17] consists of one capacitor, two complementary switches placed in parallel or series, and single DC voltage gives a greater number of levels of voltages.

Multilevel inverters (MLIs) frequently employ switched capacitor techniques to provide the desired output voltage levels. Several methods for designing MLIs with switched capacitor techniques have been put forth. To explain this, let us consider a voltage boost MLI of general purpose, which consists of number of series and parallel switches to the input and output points along diodes and capacitors [18]. As in the ref [19], one should note that the intended output voltage levels can be produced by an inductor incorporated into the resonance circuit of a quasi-resonant MLI. An arrangement of repeated switching capacitor units of cross-connection at the end of two T-type circuits is useful to find out the output voltage levels [19]- [23]. The work presented in [22] pacts a DC-source cascaded H-bridge MLI. Using switched capacitor techniques, output voltage levels are achieved by substituting isolated DC voltage sources with capacitors. Series/parallel conversion inverter for a hybrid nine-level inverter is introduced [23]. This inverter can increase voltage levels while passively balancing capacitor voltage to maintain a steady voltage. In [24], a generalized inverter topology with an active neutral point clamped (ANPC) gain1 is shown. By adding switches and capacitors, various voltage levels can be enabled. The authors of the work [23]- [26] are presented with a generic five-level inverter to increase the number of output voltage levels as compared to the earlier level inverters and which consists of four switches and a capacitor module.

Several novel multilevel inverter (MLI) topologies have been put forth in an effort to solve the problems that arise in applications involving renewable energy. The ref [25] demonstrates a hybrid T-type nine-level inverter with triple gain, in which it uses special arrangements of switches, diodes, and capacitors to provide the required voltage levels. Another invention that was introduced in [26] is the generalized CGSC-TL architecture, which provides various configurations of switches, diodes, and capacitors to generate the required voltage levels. By modifying the boost converter as an MLI using series/parallel combinations of switches, diodes, and capacitors, the CGT9L boost inverter—which was first announced in [27]-provides common grounding between the DC source and the output AC. Furthermore, the method discussed in the ref [28] creates output levels by fusing two units: an H-bridge unit and a generating unit with circuit components. A 7-level SC (7-LSC) architecture with gain-3 was introduced in [29], a MLI topology with switches of unipolar in bi-directional and bipolar in unidirectional direction was offered in [30]. Because the capacitors are naturally capable of self-balancing voltage, these topologies do not command sensor units to sense and assess the voltage between different capacitors [30]- [34]. This research concludes with the introduction of a new topology that has fewer components than current competitor topologies.

The following points indicate the contributions of the manuscript:

- A 9-level SC based MLS topology is advised with a fewer number of switches and capacitors and simulated the same by utilizing MATLAB.
- A self-balancing scheme for capacitors is introduced with a phase disposition PWM control strategy.

2. Proposed inverter topology

As shown in Figure 1, the inverter consists of mainly a source of DC voltage, capacitor numbers-two (C_1 , C_2), and electronic switches of eight. One of the switches operates bidirectionally (S_6), while the remaining seven switches function unidirectionally (S_1 to S_8).

The switches S_7 , S_8 , S_1 , and S_2 work together to prevent short-circuit damage between the source and capacitors. The C_1 and C_2 are charging and discharging in parallel and series with the DC voltage source ensures the desired output voltages. Particularly, self-balanced voltages across capacitors C_1 and C_2 are produced by charging and discharging them to $+1V_{dc}$ and $+2V_{dc}$, respectively. Across the load, the output voltage levels can be ± 1 to $\pm 4V_{dc}$. Capacitors are charged and discharged using the earlier stated techniques of parallel/series, which guarantee capacitors in balanced mode and achieve the desired voltage levels using a single DC source via a precise switching pattern. To generate all voltage levels except zero, a total of six switches are continually toggled ON in conjunction with the discharged capacitor. To reach zero, turn on the 2 switches on the upper/positive sign arm or the lower/negative sign arm.

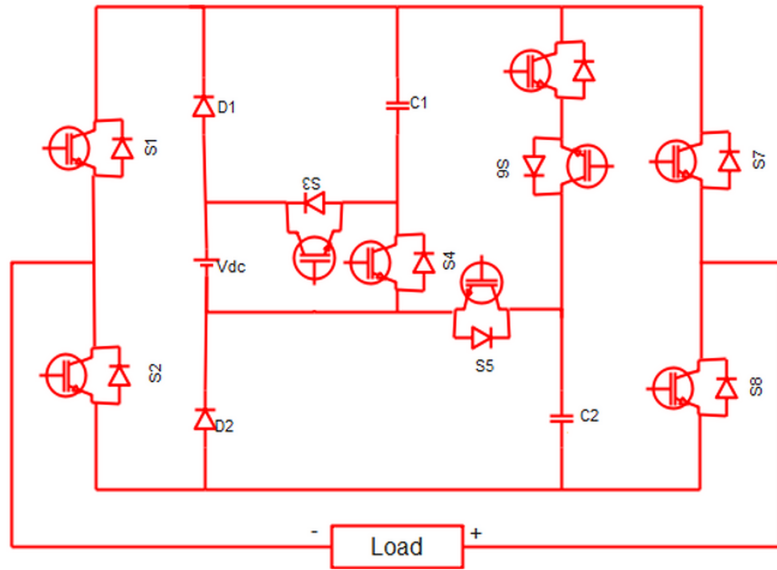


Figure 1: Architecture of proposed 9-level MLI.

2.1. Operating modes

A. Zero voltage levels:

In this work, two approaches for reaching the zero-voltage level with the suggested topology: either by turn-on the lower arm switches (S_8 , S_2) or by the upper arm switches (S_7 , S_1). The creation of the 0 V level utilizing the upper side arm switches is shown in Figure 2(a).

B. Positive voltage levels:

To achieve the different voltage levels in the proposed topology, specific switches are activated in a particular sequence. The following describes the activation of switches to generate each voltage level:

Voltage level of $+1V_{dc}$: The switches, S_7 and S_2 are activated to establish a series connection between the DC voltage source and the load. Simultaneously, switch S_4 is engaged to facilitate the charging of capacitor C_1 to $+1V_{dc}$. The C_2 is left in a floating state (-), refraining from both charging and discharging. This arrangement ensures the transmission of $+1V_{dc}$ to the load, as depicted in Figure 2(b).

Voltage level of $+2V_{dc}$: The switches, S_3 , S_7 , and S_2 are employed to create a series alignment among the DC voltage, capacitor C_1 , and the load. Additionally, switch S_3 is activated to discharge capacitor C_1 to $+1V_{dc}$, while switch S_6 is turned on to charge capacitor C_2 to $+2V_{dc}$. The outcome is the transmission of $+2V_{dc}$ to the load, as illustrated in Figure 2(c).

Voltage Level of $+3V_{dc}$: The switches S_2 , S_7 , and S_5 are activated to establish a series connection between DC voltage, capacitor C_2 , and the load. Concurrently, switch S_5 is turned on to discharge capacitor C_2 to $+2V_{dc}$. Meanwhile, capacitor C_1 remains in a floating state (-), without undergoing charging or discharging. This configuration enables the transmission of $+3V_{dc}$ to the load, as shown in figure 2(d).

Voltage Level of $+4V_{dc}$: The S_3 , S_7 , S_2 , and S_5 are activated to establish a series connection among the DC voltage, capacitor C_1 , capacitor C_2 , and the load. Switch S_3 is then turned on to discharge capacitor C_1 to $+1V_{dc}$, while switch S_4 is activated to discharge capacitor C_2 to $+2V_{dc}$. In this scenario, both capacitors release their stored energy, resulting in the transmission of $+4V_{dc}$ to the load, as depicted in figure 2(e).

C. Negative voltage levels:

To achieve negative voltage levels in the proposed topology, specific switches are activated in a particular sequence. The following describes the activation of switches to generate each negative voltage level:

Voltage Level of $-1V_{dc}$: Switches S_1 , S_8 , and S_2 are activated to establish a series connection between the DC voltage source and the load. Additionally, switch S_4 is engaged to charge capacitor C_1 to $+1V_{dc}$, while capacitor C_2 is maintained in a floating state (-), devoid of charging or discharging. This configuration facilitates the transmission of $-1V_{dc}$ to the load, as depicted in figure 2(f).

Voltage Level of $-2V_{dc}$: Switches S_3 , S_8 , and S_2 are turned on to create a series arrangement involving the DC voltage source, capacitor C_1 , and the load. Furthermore, switch S_3 is activated to discharge capacitor C_1 to $+1V_{dc}$, and switch S_6 is turned on to charge capacitor C_2 to $+2V_{dc}$. This results in the transmission of $-2V_{dc}$ to the load, as illustrated in figure 2(g).

Voltage level of $-3V_{dc}$: Activation of switches S_1 , S_8 , and S_5 establishes a series connection among the DC voltage source, capacitor C_2 , and the load. Simultaneously, switch S_5 is turned on to discharge capacitor C_2 to $+2V_{dc}$, while capacitor C_1 is kept in a floating state (-) without undergoing charging or discharging. This arrangement enables the transmission of $-3V_{dc}$ to the load, as shown in figure 2(h).

Voltage level of $-4V_{dc}$: The S_3 , S_8 , and S_5 are activated to establish a series connection involving the DC voltage source, capacitor C_1 , capacitor C_2 , and eight triangular carriers and the load. Additionally, switch S_3 is turned on to discharge the C_1 to $+1V_{dc}$, and switch S_4 is activated to discharge capacitor C_2 to $+2V_{dc}$. In this scenario, these two capacitors to deliver their earlier stored energy, resulting in the transmission of $-4V_{dc}$ to the load, as indicated in figure 2(i).

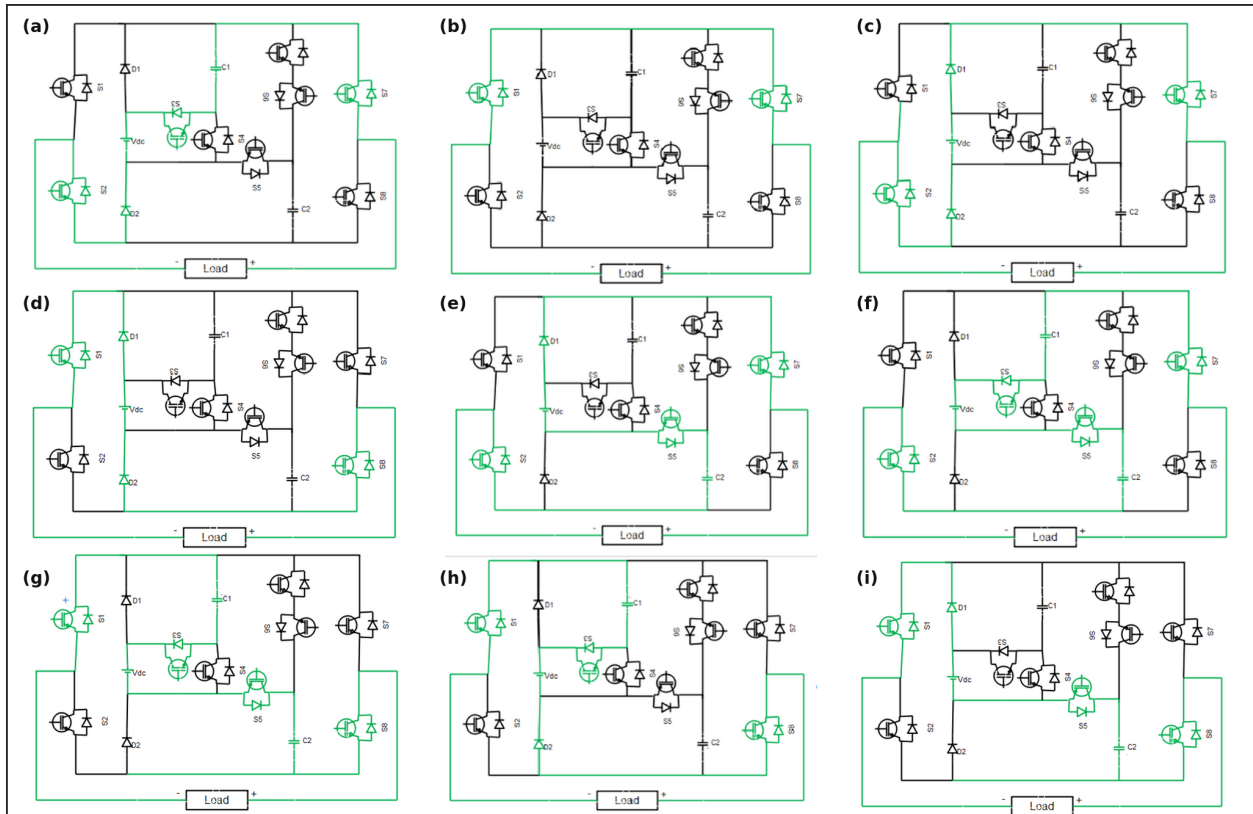


Figure 2: Operating modes of the 9-level MLI.

3. Methodology

The implementation utilizes level shifted-PWM (LS-PWM) to generate switching pulses. In this technique, the number of required carrier signals equal to the number of required level of output voltage minus one. The schema of level-shifted PWM is shown in Figure 3.

The LS-PWM employs a single sinusoidal modulating signal ($M = V_m \sin(2\pi f_m t)$) signals ($Cr_1 - Cr_8$). The comparison between the modulating signal and carrier signals generates eight pulses ($X_1 - X_8$). During positive cycles, X_1 compares M with Cr_1 , followed by X_2 comparing M with Cr_2 , and so forth. Conversely, during negative cycles, X_8 represents the comparison with Cr_8 , while X_7 compares with Cr_7 , and so on. A switching table, as outlined in Table 1, establishes the logic pattern to generate appropriate switching pulses for the switches. One should note that the value of carrier signal amplitude remains constant, while the modulation signal amplitude adjusting from 0 to 4, facilitating the generation of various modulation index values ($M_a = 0.4, 0.7$, and 0.9).

Table 1: ON and OFF stages of switching stages.

Switches (S_1 to S_8)	Output voltage levels								
	$+4V_{dc}$	$+3V_{dc}$	$+2V_{dc}$	$+V_{dc}$	$0V_{dc}$	$-V_{dc}$	$-2V_{dc}$	$-3V_{dc}$	$-4V_{dc}$
1	0	0	0	0	1	1	1	1	1
2	1	1	1	1	0	0	0	0	0
3	1	0	1	0	0	0	1	0	1
4	0	1	0	1	0	1	0	1	0
5	1	1	0	0	0	0	0	1	1
6	0	0	1	0	0	0	1	0	0
7	1	1	1	1	1	0	0	0	0
8	0	0	0	0	0	1	1	1	1

For a given value of M_a , the frequency of modulating signal resides at a constant, while the frequency of carrier signal varies between the frequencies of 125 Hz, 150 Hz, and 200 Hz to align with the load frequency of 50 Hz. Increasing the carrier signal frequency raises harmonic levels; however, to mitigate switching losses, the carrier frequency is limited to 5 KHz.

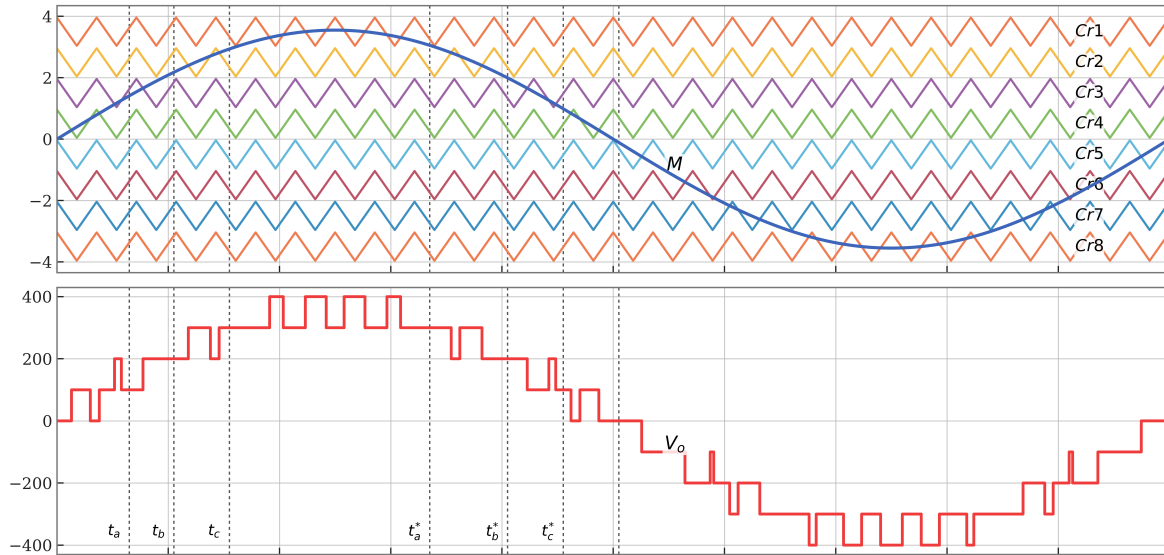


Figure 3: Schema of level-shifted PWM.

The estimation of capacitance values is imperative and that ensures the desired voltage of output under-appreciated ripple values. The output voltage levels are determined by the amount of capacitor energy, which includes charging and discharging. As illustrated in Figure 3, the calculations procedure for capacitance values are considered by considering the maximum discharging intervals. The capacitor C_1 is designed to deliver the $\pm 2V_{dc}$ and $\pm 4V_{dc}$, while the capacitor C_2 discharges at a value of $\pm 3V_{dc}$ and $\pm 4V_{dc}$. As shown in Figure 3, the switching transitions, i.e., t_a , t_b , t_c , t_a^* , t_b^* , and t_c^* for each voltage level are calculated by (1)-(6) [30]- [32].

Table 2: Comparison of the proposed topology with existing topologies.

Parameters	References													
	2012 [14]	2013 [15]	2014 [16]	2014 [17]	2017 [18]	2018 [19]	2019 [20]	2021 [24]	2021 [25]	2022 [26]	2022 [27]	2022 [28]	2022 [29]	Proposed
N_s	1	1	1	1	1	1	1	1	1	1	1	1	1	1
N_{sw}	13	12	8	10	10	17	18	12	14	9	12	10	11	8
$N_{drivers}$	13	12	8	10	10	17	18	11	14	9	12	10	11	8
N_D	0	2	6	3	4	0	5	2	0	2	1	0	0	2
N_C	3	2	3	3	3	4	4	4	5	5	2	2	2	2
G	4	4	4	4	4	1	4	3	4	4	4	4	3	4
MBV	4	4	4	4	4	4	4	3	4	2	4	4	3	4
TSV	6.25	6.25	8	6.25	7.5	7.25	7	7.5	7.5	10	7.5	6.25	5.53	6.25
N_{total}	16	16	17	16	18	21	27	18	19	16	14	12	13	12
No. of voltage levels	9	9	9	9	9	9	9	9	9	9	9	9	7	9
Efficiency (%)	85.9	83	91.5	91.6	93.5	NA	92.5	94.5	98.3	94	87–95.5	97	98.77	96.5

$$t_a = \frac{\sin^{-1}\left(\frac{1}{4}\right)}{\omega_m} \quad (1)$$

$$t_b = \frac{\sin^{-1}\left(\frac{2}{4}\right)}{\omega_m} \quad (2)$$

$$t_c = \frac{\sin^{-1}\left(\frac{3}{4}\right)}{\omega_m} \quad (3)$$

$$t_a^* = \frac{\pi - \sin^{-1}\left(\frac{1}{4}\right)}{\omega_m} \quad (4)$$

$$t_b^* = \frac{\pi - \sin^{-1}\left(\frac{2}{4}\right)}{\omega_m} \quad (5)$$

$$t_c^* = \frac{\pi - \sin^{-1}\left(\frac{3}{4}\right)}{\omega_m} \quad (6)$$

Under resistive load circumstances, the highest discharging occurs at the $\pm 4V_{dc}$ voltage level. A substantial amount of voltage decline occurs within the time interval $(t_x - t_y)$. When determining the capacitance values, careful consideration is given to extended discharging time intervals for each capacitor. It is noted that the charge or discharge cycles can occur multiple times within the $(t_x - t_y)$ interval. The discharging time intervals for capacitor C_1 are denoted as $(t_{x1} - t_{x2})$, while the corresponding intervals for capacitor C_2 are expressed as $(t_{y1} - t_{y2})$.

4. Results and discussions

The merit of the present configuration can be substantiated through simulation outcomes, considering various component parameters under diverse load conditions. Specifically, the input fix at 100 V DC, and the capacitor values are designated as $C_1 = 2200 \mu F$ and $C_2 = 2200 \mu F$. The load at end side is as $R_L = 100 \Omega + 150 \text{ mH}$ with a M_a value of 1. Figure 4 indicates (from top to bottom) the MATLAB results of output responses such as voltages and currents. Figures Figure 4 and Figure 5 represent simulation results corresponding to output voltage, current and capacitor voltages under RL load and the switching frequency variations.

Table 2 provides a comprehensive comparison of various parameters across multiple references in the literature. The parameters include N_s (no. of stages), N_{sw} (no. of switches), $N_{drivers}$ (no. of drivers), N_D (no. of diodes), N_C (no. of capacitors), G (Gain), MB (Minimum breakdown voltage), TSV (Total simulation time in milliseconds), N_{Total} (Total number of components), Number of Voltage Levels, and Efficiency (%). Each parameter is compared across different references spanning from 2012 to proposed solutions, with corresponding numerical values provided for each reference year. The table offers insights into the evolution and performance variations of different solutions over time, allowing researchers and practitioners to analyze trends and make informed decisions regarding the selection and optimization of circuit designs. Additionally, the efficiency percentages provide an indication of the overall effectiveness of the solutions, with higher values suggesting improved performance and energy utilization. This comparative analysis aids in identifying potential areas for further research and improvement in the design and implementation of electrical circuits.

The proposed configuration exhibits the capability to elevate the input voltage from 100 V to 400 V as voltage at output while maintaining equilibrium in capacitor voltages with C_1 at 100 V and C_2 at 200 V. The voltage THD of the output is recorded below 5%.

5. Conclusion

This article introduces a brand-new nine-level inverter with a single DC supply that is intended for standalone solar PV installations. The suggested topology uses a parallel/series-charging/discharging method for capacitors and boasts quadruple voltage gain capabilities. The voltages of capacitors are balanced using LSPWM to produce the desired output voltage with the least amount of component stress. This topology's experimental setup can be adjusted to accommodate a range of situations, such as changing load scenarios, variation of input voltage, switching frequency, changes in amplitude and frequency modulation and frequency adjustments. Both the output voltage's THD and the capacitors' voltage ripples fall well within permissible bounds of 5%. A comparative study shows that the suggested topology has a simple structure, fewer switches, the ability to boost quadruple, improved efficiency, affordability, and a lower Total Switching Stress (T.S.V). Results from MATLAB simulations support the effectiveness of the suggested design. Essentially, this novel topology provides a single DC source power solution for renewable solar PV applications that need triple voltage gain DC-AC power conversion and less switching stress from fewer switches. The current work can be extended to emerging areas of RES and electric vehicles [35]–[38].

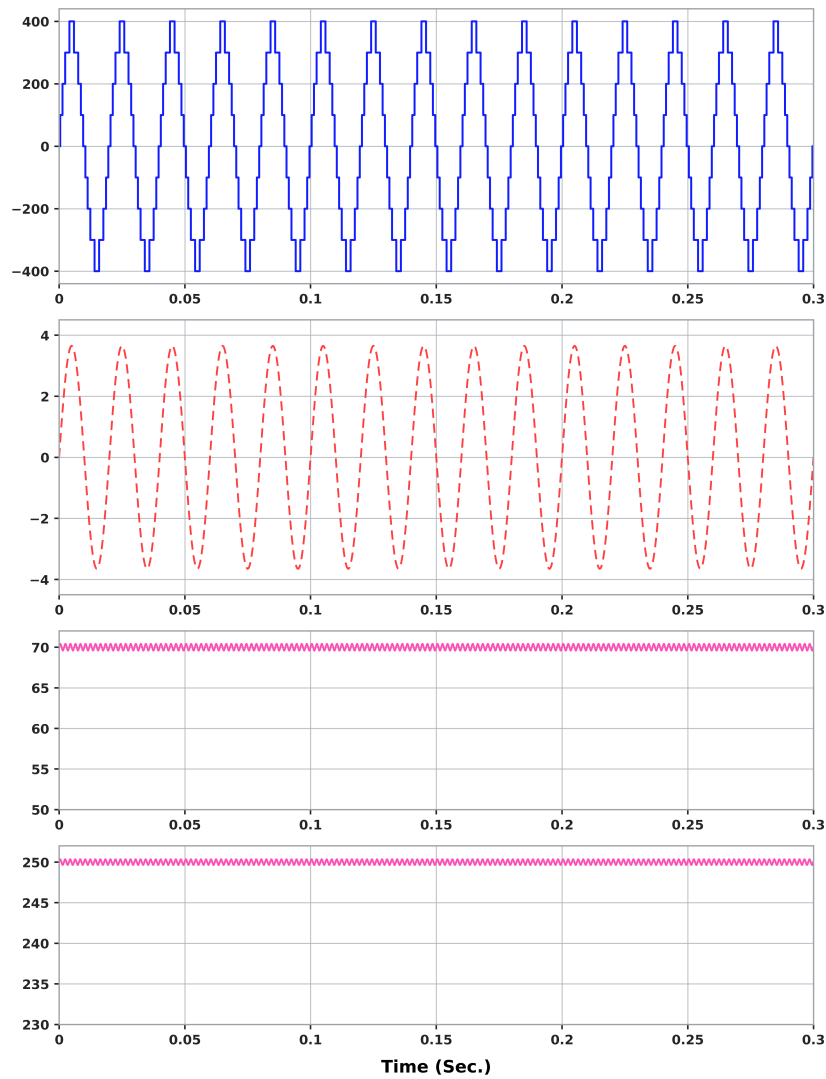


Figure 4: Output responses of (a) voltage, (b) current and (c) capacitor for RL load.

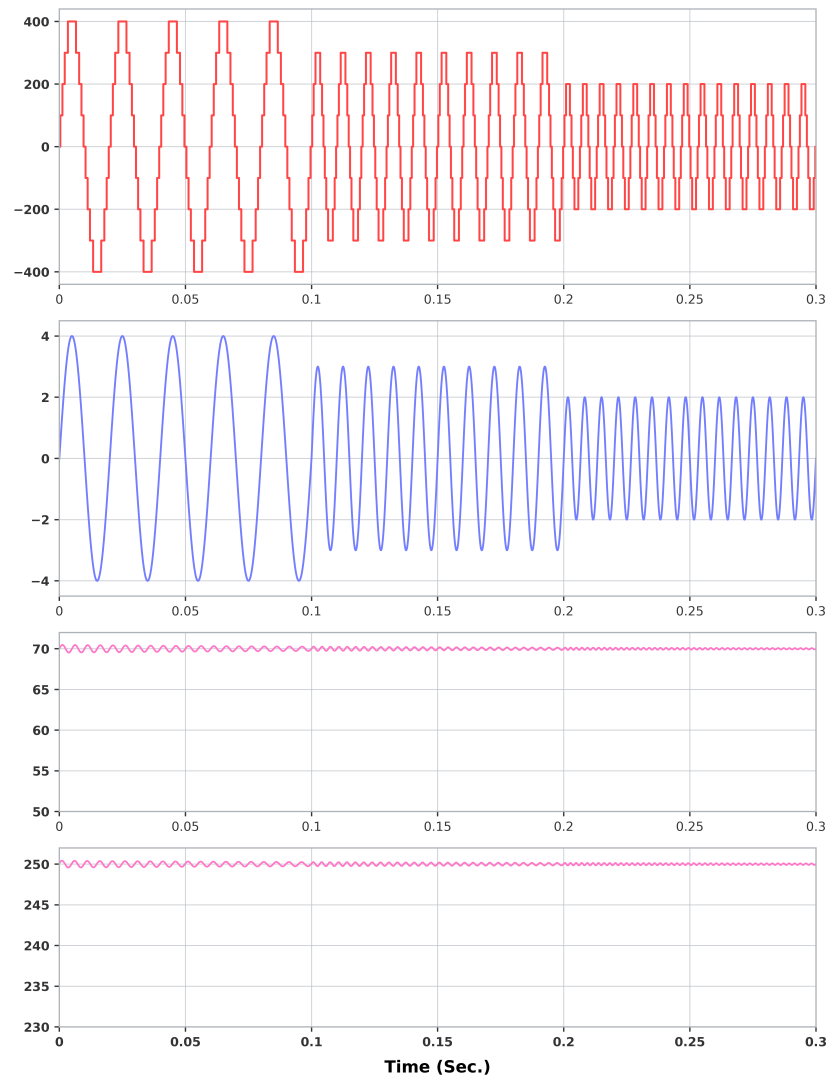


Figure 5: Output responses (top to bottom) of output voltage, current and capacitor voltage across capacitors.

Declarations and ethical statements

Conflict of interest: The authors declare that there is no conflict of interest.

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Artificial Intelligence usage statement: During the preparation of this manuscript, the authors utilized ChatGPT solely for language refinement and grammatical corrections. The authors carefully reviewed and revised the generated content and take full responsibility for the accuracy, integrity, and originality of the final manuscript.

Availability of data and materials: The paper uses secondary data and the same has been cited in the paper.

CRedit authorship contribution statement

Lois Anuale: Conceptualization, Implementation, Methodology, Visualization, Validation, Writing–Original draft, Review & Editing. **Osasumwen J. T. Alimikhena:** Methodology, Writing–Original draft, Review & Editing. **Olafuyi Ogunmuyiwa:** Formal analysis & Visualization.

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